IN THE CLAIMS:

1.-10. (Canceled)

11. (Currently Amended) A method, comprising:

forming a dielectric mask region above a P-doped semiconductor layer formed on an insulating substrate; and

forming a P-doped region and an N-doped region in said P-doped semiconductor layer, said P-doped region and said N-doped region being self-aligned with respect to said dielectric mask region, wherein ~~using said dielectric mask region to create~~ a PN-junction is created between the P-doped semiconductor layer ~~region~~ and the N-doped region below said dielectric mask region.

12. (Original) The method of claim 11, further comprising forming silicide regions in said P-doped and N-doped regions, wherein said dielectric mask region prevents a short between the P-doped region and the N-doped region.

13. (Original) The method of claim 11, further comprising forming an insulating layer on said semiconductor layer, wherein said dielectric mask region is formed on said insulating layer.

14. (Original) The method of claim 11, further comprising adjusting a width of said dielectric mask region so as to control a dopant gradient towards said PN-junction.

15. (Original) The method of claim 14, wherein said width is in the range of approximately 0.03-0.2 μm.

16. (Original) The method of claim 11, wherein forming said P-doped region and said N-doped region includes forming a resist mask to cover a first portion and expose a second portion of said semiconductor layer and to partially cover said dielectric mask region.

17. (Original) The method of claim 16, further comprising implanting N-type dopants into said second portion to form the N-doped region.

18. (Original) The method of claim 17, further including forming a second resist mask to cover said second portion and expose said first portion of said semiconductor layer and to partially cover said dielectric mask region.

19. (Original) The method of claim 18, further comprising implanting P-type dopants into said first portion to form the P-doped region.

20. (Original) The method of claim 11, further comprising forming a first contact plug, connecting to said P-doped region, and forming a second contact plug, connecting to said N-doped region.

21. (Original) The method of claim 11, wherein said P-doped region and said N-doped region are arranged in a side-by-side configuration.

22. (Original) The method of claim 11, wherein one of said P-doped region and said N-doped region is arranged to at least partially enclose the other one of said P-doped region and said N-doped region.

23. (Original) The method of claim 11, further comprising forming a transistor structure in said semiconductor layer.

24. (Original) The method of claim 23, further comprising forming a halo implantation mask that at least covers a first portion and a second portion of said semiconductor layer prior to forming said P-doped region and said N-doped region in said first and second portions, respectively.

25. (New) A method, comprising:

forming a dielectric mask region above a P-doped semiconductor layer on an insulating substrate; and

forming a P-doped region and an N-doped region in said P-doped semiconductor layer wherein a PN junction is created between said N-doped region and said P-doped semiconductor layer, wherein forming said N-doped region comprises:

forming a first resist mask above said P-doped semiconductor layer and at least a portion of said dielectric mask region to thereby define a first exposed portion of said P-doped semiconductor layer; and

performing at least one ion implant process to implant an N-type dopant material into said first exposed portion of said P-doped semiconductor layer.

26. (New) The method of claim 25, wherein said P-doped region and said N-doped region are self-aligned with respect to said dielectric mask region.

27. (New) The method of claim 25, wherein forming said P-doped region comprises:

forming a second resist mask above said P-doped semiconductor layer and at least a portion of said dielectric mask region to thereby define a second exposed portion of said semiconductor layer; and

performing at least one ion implant process to implant a P-type dopant material into said second exposed portion of said P-doped semiconductor layer.

28. (New) The method of claim 25, further comprising forming silicide regions in said P-doped and N-doped regions, wherein said dielectric mask region prevents a short between the P-doped region and the N-doped region.

29. (New) The method of claim 25, further comprising forming an insulating layer on said semiconductor layer, wherein said dielectric mask region is formed on said insulating layer.

30. (New) The method of claim 25, further comprising adjusting a width of said dielectric mask region so as to control a dopant gradient towards said PN-junction.

31. (New) The method of claim 30, wherein said width is in the range of approximately 0.03-0.2 μm.

32. (New) The method of claim 25, further comprising forming a first contact plug, connecting to said P-doped region, and forming a second contact plug, connecting to said N-doped region.

33. (New) The method of claim 25, further comprising forming a transistor structure in said semiconductor layer.

34. (New) A method, comprising:

forming a dielectric mask region above an N-doped semiconductor layer formed on an insulating substrate; and

forming a P-doped region and an N-doped region in said N-doped semiconductor layer, said P-doped region and said N-doped region being self-aligned with respect to said dielectric mask region, wherein a PN-junction is created between the N-doped semiconductor layer and the P-doped region below said dielectric mask region.

35. (New) The method of claim 34, further comprising forming silicide regions in said P-doped and N-doped regions, wherein said dielectric mask region prevents a short between the P-doped region and the N-doped region.

36. (New) The method of claim 34, further comprising forming an insulating layer on said semiconductor layer, wherein said dielectric mask region is formed on said insulating layer.

37. (New) The method of claim 34, further comprising adjusting a width of said dielectric mask region so as to control a dopant gradient towards said PN-junction.

38. (New) The method of claim 37, wherein said width is in the range of approximately 0.03-0.2 μm.

39. (New) The method of claim 34, wherein forming said P-doped region and said N-doped region includes forming a resist mask to cover a first portion and expose a second portion of said semiconductor layer and to partially cover said dielectric mask region.

40. (New) The method of claim 39, further comprising implanting N-type dopants into said second portion to form the N-doped region.

41. (New) The method of claim 40, further including forming a second resist mask to cover said second portion and expose said first portion of said semiconductor layer and to partially cover said dielectric mask region.

42. (New) The method of claim 41, further comprising implanting P-type dopants into said first portion to form the P-doped region.

43. (New) The method of claim 34, further comprising forming a first contact plug, connecting to said P-doped region, and forming a second contact plug, connecting to said N-doped region.

44. (New) The method of claim 34, wherein said P-doped region and said N-doped region are arranged in a side-by-side configuration.

45. (New) The method of claim 34, wherein one of said P-doped region and said N-doped region is arranged to at least partially enclose the other one of said P-doped region and said N-doped region.

46. (New) The method of claim 34, further comprising forming a transistor structure in said semiconductor layer.

47. (New) The method of claim 46, further comprising forming a halo implantation mask that at least covers a first portion and a second portion of said semiconductor layer prior to forming said P-doped region and said N-doped region in said first and second portions, respectively.

48. (New) A method, comprising:

forming a dielectric mask region above an N-doped semiconductor layer on an insulating substrate; and

forming a P-doped region and an N-doped region in said N-doped semiconductor layer wherein a PN junction is created between said P-doped region and said N-doped semiconductor layer, wherein forming said P-doped region comprises:

forming a first resist mask above said N-doped semiconductor layer and at least a portion of said dielectric mask region to thereby define a first exposed portion of said N-doped semiconductor layer; and

performing at least one ion implant process to implant a P-type dopant material into said first exposed portion of said N-doped semiconductor layer.

49. (New) The method of claim 48, wherein said P-doped region and said N-doped region are self-aligned with respect to said dielectric mask region.

50. (New) The method of claim 48, wherein forming said N-doped region comprises:

forming a second resist mask above said N-doped semiconductor layer and at least a portion of said dielectric mask region to thereby define a second exposed portion of said N-doped semiconductor layer; and

performing at least one ion implant process to implant an N-type dopant material into said second exposed portion of said N-doped semiconductor layer.

51. (New) The method of claim 48, further comprising forming silicide regions in said P-doped and N-doped regions, wherein said dielectric mask region prevents a short between the P-doped region and the N-doped region.

52. (New) The method of claim 48, further comprising forming an insulating layer on said semiconductor layer, wherein said dielectric mask region is formed on said insulating layer.

53. (New) The method of claim 48, further comprising adjusting a width of said dielectric mask region so as to control a dopant gradient towards said PN-junction.

54. (New) The method of claim 53, wherein said width is in the range of approximately 0.03-0.2 μm.

55. (New) The method of claim 48, further comprising forming a first contact plug, connecting to said P-doped region, and forming a second contact plug, connecting to said N-doped region.

56. (New) The method of claim 48, further comprising forming a transistor structure in said semiconductor layer.